CLAIMS

1. A video display controller, comprising:

a memory unit that receives display data from an external bus and temporarily stores the display data;

a data converter connected to the memory unit for receiving the display data therefrom and converting the display data to a converted data having a predetermined format;

a display data generator connected to the data converter for receiving the converted data and generating temporary display data therefrom using a predefined algorithm;

a holding register connected to the display data generator for storing the generated temporary display data; and

a multiplexer connected to the data converter for receiving the converted data and the holding register for receiving the generated temporary display data, wherein the multiplexer selects and outputs one of the converted data and the generated temporary display data in accordance with a bus overload signal that indicates a predetermined condition of the external bus.

2. The video display controller of claim 1, further comprising an interface logic unit connected to the multiplexer for receiving the multiplexer output signal and reformatting the multiplexer output signal in accordance with a predetermined display format.

3. The video display controller of claim 2, wherein the video display controller is connected to a liquid

crystal display and the interface logic unit formats the multiplexer output signal to a predetermined LCD format.

4. The video controller of claim 1, wherein the memory unit includes a DMA controller and a FIFO memory, wherein the DMA controller is connected between the external bus and the FIFO memory and the DMA controller receives the display data from the external bus and stores the received data in the FIFO memory.

5. The video controller of claim 4, wherein the bus overload signal is derived from the read and write pointers of the FIFO memory.

6. The video controller of claim 1, wherein the bus overload signal indicates a bus overload condition.

7. The video controller of claim 1, wherein the data converter performs modulation and dithering operations, and color mapping using a palette table on the stored display data.

8. The video controller of claim 1, wherein the predefined algorithm comprises breaking a current line of the converted display data into subgroups and calculating an average using the subgroup bits to generate bits of the temporary display data.

9. The video controller of claim 1, wherein the predefined algorithm comprises breaking a current line of the converted display data into subgroups and calculating a majority using the subgroup bits to generate bits of the temporary display data.

10. The video controller of claim 1, wherein the holding register is sized to store at least one word of the generated display data.

11. A LCD controller that receives display data from an external bus and provides modified display data to an LCD, the LCD controller comprising:

a DMA controller connected to the external bus for fetching and receiving display data transmitted over the external bus;

a FIFO memory connected to the DMA controller for receiving and temporarily storing the display data;

a data converter connected to the FIFO memory for receiving the display data therefrom and converting the display data to converted data having a predetermined format;

a display data generator connected to the data converter for receiving the converted data and generating temporary display data therefrom using a predefined algorithm;

a holding register connected to the display data generator for storing the generated temporary display data;

a multiplexer connected to the data converter for receiving the converted data and the holding register for receiving the generated temporary display data, wherein the multiplexer selects and outputs one of the converted data and the generated temporary display data in accordance with a bus overload signal that indicates a predetermined condition of the external bus; and

an interface logic unit connected to the multiplexer for receiving the multiplexer output signal and reformatting the multiplexer output signal in accordance with a

predetermined display format and providing the reformatted output signal to the LCD.

12. The video controller of claim 11, wherein the predefined algorithm comprises breaking a current line of the converted display data into subgroups and calculating an average using the subgroup bits to generate bits of the temporary display data.

13. The video controller of claim 11, wherein the predefined algorithm comprises breaking a current line of the converted display data into subgroups and calculating a majority using the subgroup bits to generate bits of the temporary display data.

14. A method of processing display data received from a bus and provided to a LCD, the method comprising the steps of:

receiving display data from an external bus and storing the received display data in a memory unit;

reading the display data stored in the memory unit;

converting the read display data to a predetermined format;

providing the formatted display data to a first input of a multiplexer and to a display data generator;

the display data generator generating temporary display data using the formatted display data in accordance with a predefined algorithm;

storing the generated temporary display data in a holding register;

providing the temporary display data from the holding register to a second input of the multiplexer;

selecting by the multiplexer one of the formatted display data and the generated temporary display data in accordance with a bus overload signal; and

outputting the selected data to a display device.

15. The method of processing display data of claim 14, wherein the predefined algorithm comprises breaking a current line of the converted display data into subgroups and calculating an average using the subgroup bits to generate bits of the temporary display data.

16. The method of processing display data of claim 14, wherein the predefined algorithm comprises breaking a current line of the converted display data into subgroups and calculating a majority using the subgroup bits to generate bits of the temporary display data.